Synthesis of Si Nanostrutures via Self-organized Pillar Mask

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Recently, nanodot arrays have attracted a great deal of attention because of their realization in functional structures and in the field of nanodevices such as optoelectronics, information storage, and sensing.[1−5] Although lithographic techniques offer good control over nanodot size, shape, and spacing, these techniques include expensive and time-consuming processes. Therefore, a variety of alternative methods have been proposed for the formation of nanodot arrays on substrates, including self-assembly of nanodots from solution onto a substrate,[6] strain-induced growth,[7] and template-based methods.[8] However, most of these works can be applied to only limited material systems. In this report, we demonstrate an efficient method for fabricating nanodot arrays by using self-organized etching masks based on oxide pillar formation at the bottom of anodic alumina templates (AAT). Our method can be applied to a wide range of materials and over a large area. By forming self-organized oxide pillar arrays and direct patterning to the underlying films using oxide pillar arrays, we can prepare the desired nanodot arrays on the substrate.

Figure 1 depicts the schematic of the overall process for the fabrication of Si nanodot arrays onto a wafer. Our approach is based on a well-known aluminum anodization technique, which results in densely packed pore formation.[9] Our strategy begins with the preparation of a layered structure of Al/Ta/Si on a thermally oxidized Si wafer. A sputtered Si film was first prepared on the thermally oxidized wafer, followed by successive deposition of Ta and Al films also by dc sputtering as shown in Figure 1a. Two anodization conditions were chosen to prepare the different sizes of self-organized tantalum oxide hard masks. One was for a relatively large hard mask. The other was for the smaller etching mask. After full anodization of the Al layer, the underlying Ta layer was anodized, resulting in the formation of tantalum oxide pillar arrays at the bottom of AAT. Selective removal of the porous alumina layer by chemical etching is performed to reveal tantalum oxide pillar arrays. Finally, direct pattern transfer to the underlying Si films results in the formation of Si nanodot arrays on the wafer as shown in Figure 1c,d.

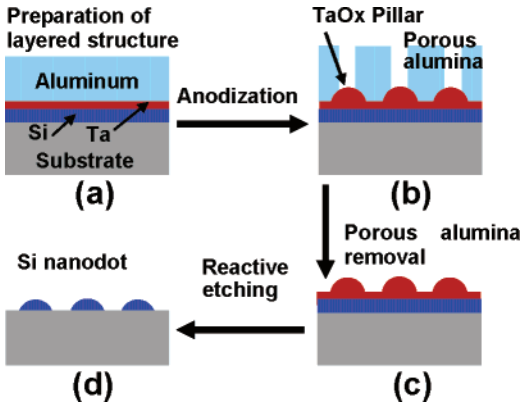

Figure 1. Process for fabricating Si nanodot arrays by using self-organized tantalum oxide as a hard mask. (a) Preparation of layered structure; (b) formation of tantalum oxide pillar arrays through Al anodization; (c) removal of porous alumina layer; (d) reactive ion etching to form Si nanostructures.

Initially, anodizing was performed to form a self-organized tantalum oxide pillar mask at the bottom of AAT pores. As the anodization proceeds, an array of pores develops on the thin, nonporous film of Al_2O_3, whose diameter grows until reaching steady-state conditions. At steady state, the Al_2O_3 dissolution at the Al_2O_3/electrolyte interface, which is located at the bottom of the pores, is in equilibrium with the Al_2O_3 oxide growth at the Al_2O_3/Al interface with forming straight pores. As the growing pores approach the Ta layer, electrochemical anodization of the Ta layer begins. The anodic reaction of Ta results in the formation of tantalum oxide accompanied by formation of hemispherical structures due to volume expansion (Figure 1b). Experimental details and the mechanism of the tantalum oxide formation at the bottom of AAT during the anodization process of the Al/Ta layer were previously reported by Vorobyova and co-workers.[10a] Figure 2a show a cross-sectional transmission electron microscopy (TEM) image of the AAT after full anodization. The TEM image clearly shows that there are grown pillar arrays at the interface between the bottom of the AAT pore and initially deposited Ta layer. The thickness of the anodized metal film depends on applied voltage and is usually quoted in terms of the anodizing ratio

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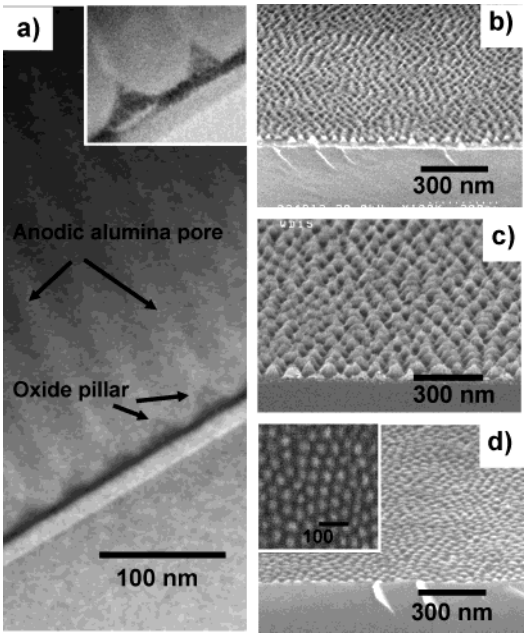

Figure 2. TEM image of (a) cross-sectional views of tantalum oxide pillar arrays formed at the bottom of porous alumina template and SEM images of (b) tantalum oxide pillar arrays with 31-nm diameter, (c) tantalum oxide pillar arrays with 90-nm diameter, and (d) Si nanodot arrays. Inset in (a): enlarged view of tantalum oxide pillars. Inset in (d): top view of ordered Si nanodot arrays.

(thickness of oxide formed per unit applied voltage, Å/V). The anodizing ratio of tantalum is 16.0. The possible thickness of the tantalum oxide at an applied voltage of 19 and 40 V is 30.4 and 64 nm, respectively. The Pilling-Bedworth ratio, which is defined as the ratio of $V_{\text{metal oxide produced}}/V_{\text{metal consumed}}$, of Ta is 2.33. In this context, it is reasonable to assume that the 4-nm-thick Ta layer in our samples is fully oxidized without any remaining Ta metal. This explanation is in good agreement with the energy-dispersive X-ray (EDX) results. EDX spectra taken at pillar structures revealed that the pillar structure formed at the bottom of an AAT consisted of tantalum oxide. The chemical characteristics and shape of the pillar structure indicate electrochemical oxidation proceeded by preferential oxidation of tantalum at the bottom of alumina pores. After the full anodization of Al/Ta layers, the resulting porous alumina films were removed by wet chemical etching in a mixed solution of H_3PO_4 and CrO_3. Thus, tantalum oxide pillar arrays were produced on the surface of the Si layer. Figure 2b,c shows field-emission scanning electron microscopy (FE-SEM) images of tantalum oxide pillar arrays formed at the bottom of AAT after removal of the porous alumina. The close-packed and cone-shaped structure is clearly seen over a quite large area of the samples. The self-organized nanopillar arrays of tantalum oxide have an average diameter of about 90 and 31 nm, respectively, which is relatively larger than the pore size of the AAT. The corresponding pore sizes of AAT were 33 and 12 nm, respectively. It may be due to the radial anodizing field distribution at the Ta layer,[10] after AAT pores reach the Ta layer. This field distribution results in the oxidation of tantalum toward the tantalum oxide pillar tips rather than perpendicularly across the film section, forming larger diameter of cone-shaped tantalum oxide pillars than that of the AAT pores. From the observation of the pillar structures by FE-SEM, it has been found that the height of pillar arrays is constant over the entire surface and is determined by the value of the initial thickness of the Ta layer and the anodizing conditions. The densities of tantalum oxide pillar were approximately $1.0 \times 10^{10}/\text{cm}^2$ and $3.8 \times 10^{10}/\text{cm}^2$, which is in good agreement with the pore density of the AAT.

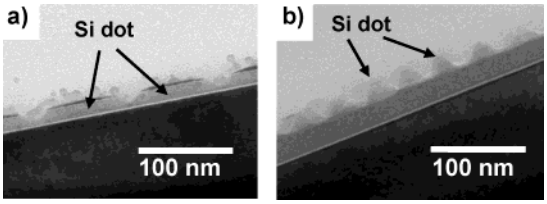

Figure 3. Cross-sectional TEM images of (a) Si nanodot arrays with 90-nm diameter and (b) Si nanopillar arrays with 31-nm diameter. For the fabrication of different sizes of dot arrays, two anodizing conditions were chosen. Selected anodization conditions were applied voltage of 40 V in a 0.1 M oxalic acid solution and 19 V in 0.1 M sulfuric acid solution for (a) and (b) respectively.

As a next step, tantalum oxide pillar arrays were used as hard masks for the subsequent transfer of oxide nanopillar arrays into an underlying Si layer. The pattern transfer is carried out by reactive ion etching (RIE) in Cl_2 plasma by varying the etching time (10−80 s) under a coil rf power of 600 W and a dc-bias voltage of 150 V. The pressure was 5 mTorr. The selectivity (the ratio of tantalum oxide etch rate/silicon etch rate) is approximately 0.5, which ensures the preservation of the pattern during the RIE process. The etching rates for the tantalum oxide pillar and the underlying Si layer were about 50 and 100 nm/min, respectively. The results of pattern transfer after the RIE process are shown in Figure 2d and Figure 3. As shown in Figure 2d, direct pattern transfer of tantalum oxide pillar arrays onto the Si layer is clearly evident over the large area: The conical shape and areal density of Si dot arrays coincide with those of tantalum oxide pillar mask. Figure 3a,b shows a cross-sectional view of relatively large diameter Si dot arrays with tantalum oxide caps (dark line at the top of dot) and relatively small diameter Si pillar arrays without tantalum oxide caps after the RIE process. TEM analysis and EDX spectra confirmed the presence or absence of tantalum oxide caps.

One can prepare Si nanodot and pillar arrays as shown in Figure 3 by suitable choice of the initial thickness of Si layer and RIE conditions. Figure 3a,b shows 90-nm Si nanodot arrays and 31-nm Si nanopillar arrays, respectively. The fabrication of an array of Si nanodots could be achieved in nanometer dimensions over a wide range of possible substrates as well as over a large area. The dimensions of the tantalum oxide pillar arrays used as an etching mask are dependent on the anodizing conditions. Such nanodot arrays with an adjustable diameter and areal density are suitable for desired applications. It is expected that the novel technique presented here is not limited to specific materials for preparing nanodot arrays on a substrate.

Because the aluminum layers in our study were only about 500 nm, the tantalum oxide pillar at the bottom of AAT were not highly ordered. It might be possible to obtain a more ordered tantalum oxide pillar mask with

a narrower size distribution by starting with thicker Al films,[8] which would result in highly ordered Si dot arrays. Alternatively, anodization after indenting the Al surface with a concave mold[11] enables us to prepare highly ordered Si nanodot arrays with narrower size distribution. We also expect that an additional oxidation[12] and etching process for the formed Si nanodots would reduce the size of the Si nanodots.

In conclusion, we have demonstrated an efficient method for fabricating Si nanodot/pillar arrays by using a self-assembled mask based on tantalum oxide pillar formation at the bottom of an AAT. The process allows high-density arrays of nanodots to be prepared. The nanodot density demonstrated here is above $10^{10}/cm^2$. In addition, dot size and density can be controlled through the choice of anodization conditions. The controllable self-organization process of forming the nanodot etching mask and pattern transfer offers a simple and nonexpensive way to fabricate a variety of low-dimensional nanodot arrays on Si wafers over a large area.

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Supporting Information Available: Experimental details (PDF). This material is available free of charge via the Internet at http://pubs.acs.org.

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